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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/662,977	09/15/2003	Dong-yang Lee	8021-165 (SS-17922-US)	2257

22150 7590 02/09/2006

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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/662,977	LEE, DONG-YANG	
	Examiner	Art Unit	
	Alan S. Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/06/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by US Pat. No. 6,211,695 to Agrawal et al. (Agrawal).

3. Per claim 1, Agrawal discloses an integrated circuit device (FPGA is integrated circuit, Figs. 8-10 shows parts/components of the FPGA) comprising a first port for inputting and outputting data (Figs. 8 and 9, elements 874 and 884 are the input/output data and address ports; note these are bidirectional); a second port for inputting data (Fig. 8, elements 872 and 882 are unidirectional lines, e.g., read only; it should be noted that the claims do not specify in relation to the integrated circuit whether the data for the "input" line is data to be read out of the integrated circuit or written in. Under the broadest reasonable interpretation, the second port is simply unidirectional; the described logic in the specification for accommodating unidirectional and bidirectional functionality is directly anticipated by Agrawal), wherein at least one of the first port and the second port is selected by an external command (Fig. 9, commands are the enable signals, i.e., ROEN, R/WEN, OE in elements 934, 936 and 883) when the data is input.

4. Per claim 5, Agrawal discloses an integrated circuit system (Fig. 1A shows the high level diagram of FPGA, in essence a system on a chip) comprising: an integrated circuit device (Fig. 8, element 870 is a SRAM block) that includes a first port for inputting and outputting data (Fig.

8, element 874 and 884 is bidirectional) and a second port for inputting data (Fig. 8, elements and 872); and a controller for generating a command to select either the first port or the second port (Fig. 9, various controllers are present to determine when to enable read and write; elements 941 and 942 must be true in order for the first or second port to be selected to input/output data).

5. Per claims 9 and 16, Agrawal discloses an integrated circuit device (FPGA is integrated circuit, Figs. 8-10 shows parts/components of the FPGA) comprising a first port for inputting and outputting data (Figs. 8 and 9, elements 874 and 884 are the input/output data and address ports; note these are bidirectional); a first buffering unit in signal communication with the first port for buffering and storing the input or output data (Fig. 9, elements 974 and 975 are bidirectional buffers; Column 31, lines 55-65 expressly disclose these buffers); a second port for inputting data (Fig. 8, elements 872 and 882 are unidirectional lines, e.g., read only; a second buffering unit in signal communication with the second port for buffering and storing the input data (Fig. 9, element 964); and a selecting unit (Fig. 9, elements 950 and 942 both determine whether to allow the bidirectional read/write and unidirectional read data) for selecting outputs from at least one of the first buffering unit (Fig. 9, element 950 determines whether to output from 974 and 975) and the second buffering unit (Fig. 9, element 942 determines whether to output from buffer element 964) to output in response to a selection signal (signals ROEN, element 936 and R/WEN, element 934 enable the read/write of the buffers), wherein at least one of the first port and the second port is selected by an external command when the data is input (Fig. 3B shows that memory data goes into the SRAM block, element 472, command control lines, element 471 or 481 that enable SRAM to read/write data through its ports; Column 16, lines 43+; in addition, OE, output enable shown in Fig. 8 as external to the SRAM block controls the read/write data

port in addition to the R/WEN signals) and at least one of the first buffering unit and the second buffering unit is turned on by the external command (Fig. 9, element 883, OE must be high for buffer 974 to be enabled). Agrawal further discloses a register (Fig. 9, element 975) is a register for storing data from the I/O buffers per claim 16.

6. Per claims 2,6,10 and 17, Agrawal discloses claims 1,5,9 and 16, the ports having the same number of pins (Fig. 8, element 882 and 884 have the same number of pins/lines=4, address pins/lines, element 872 and 874 also has same number of pins/lines=5). Note the variable "n" here is equal to 0, zero by definition, being a natural number (www.wikipedia.com->natural numbers).

7. Per claims 3,4,7,8,13-15 and 18-20, Agrawal discloses claims 1,5,9 and 16, wherein both the first and second port are selected by an external command when the data is input (Fig. 9, enable signals are construed to be the command signals that select whether data is sent in/out of the ports). The enable signals are inherently sent over some contact control pin at the source to the logic gate/destination.

8. Per claims 11 and 12, Agrawal discloses claim 9, wherein both buffers have registers to store input/output data (Fig. 9, elements 921 and 976) to be output to the SRAM requestor outside of the SRAM unit (Fig. 8, element 870), the requestor being the selection unit that desired the data in the SRAM block.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Patents and patent related publications are cited in the Notice of References Cited

(Form PTO-892) attached to this action to further show the state of the art with respect to control multiport integrated circuits.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S. Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim N. Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
01/31/2006

KIM HUYNH
SUPERVISORY PATENT EXAMINER
2/2/06